WHAT IS CLAIMED IS:

1. A system for controlling radio components, said system comprising:

a microcode random access memory for storing a frame program, said frame program comprising a certain instruction;

a microsequencer for executing the certain instruction;

a microwire for transmitting a predetermined number of bytes to the radio components, responsive to the microseqeuncer executing the certain instruction; and

a delay unit for selectively delaying the microsequencer by a predetermined period of time, responsive to the microsequencer executing the certain instruction.

2. The system of claim 1, wherein the certain instruction comprises a value indicative of the predetermined number of bytes.

3. The system of claim 2, wherein the value is indicative of the predetermined period of time.

4. The system of claim 3, wherein the predetermined period of time is the value minus one.

5. The system of claim 2, further comprising:

a microwire random access memory for storing the predetermined number of bytes at a particular address; and

wherein the certain instruction comprises the particular address.

6. The system of claim 5, and wherein the value and the particular address are indicative of the predetermined period of time.

7. The system of claim 5, wherein the predetermined period of delay is the value minus one if the particular address is odd.

8. A method for controlling radio components, said method comprising:

executing a certain instruction;

transmitting a predetermined number of bytes to the radio components, responsive to executing the certain instruction; and

selectively preventing execution of other instructions for a predetermined period of time, responsive to executing the certain instruction.

9. The method of claim 8, wherein the certain instruction comprises a value indicative of the predetermined number of bytes.

10. The method of claim 9, wherein the value is indicative of the predetermined period of time.

11. The system of claim 10, wherein the predetermined period of time is the value minus one.

12. The method of claim 9, wherein the certain instruction comprises a particular memory address, and wherein transmitting a predetermined number of bytes further comprises transmitting the predetermined number of bytes beginning at the particular memory address.

13. The method of claim 12, wherein the value and the particular memory address are indicative of the predetermined period of time.

14. The system of claim 5, wherein the predetermined period of delay is the value minus one if the particular memory address is odd.

15. An apparatus for controlling radio components, said apparatus comprising a microcode random access memory storing a frame program, said frame program comprising a certain executable instruction, said certain executable instruction comprising means for:

transmitting a predetermined number of bytes to the radio components; and

selectively preventing execution of other executable instructions for a predetermined period of time.

16. The apparatus of claim 15, wherein the means for transmitting a predetermined number of bytes to the radio components further comprises means for transmitting the predetermined number of bytes to the radio components beginning at a predetermined memory address.

17. The apparatus of claim 16, wherein the means for selectively preventing execution of other executable instructions for a predetermined period of time further comprises selectively preventing execution of other executable instruction based upon the predetermined memory address.